

MCFD-16 is an easy to use fast 16 channel constant fraction discriminator (CFD) for high timing resolution applications. It provides fast amplifiers at the inputs which can be set for input polarity and gains.

The amplifier outputs are split to the CFD unit and are available as unipolar or differential signals (configurable) at an output connector. The discriminator signals are available as ECL differential outputs at a 34 pin header connector.

In differential mode, the analog outputs allow to drive long twisted pair delay cables to introduce the necessary delay needed for charge sensitive ADCs (QDCs).

A fast pattern processing is implemented, well suited to produce complex triggers from input coincidences.

### Built in fast preamplifier

- Gain 1, 3, and 10
- Polarity selectable
- 300 MHz band width
- Output configurable via Jumper: unipolar or differential

### Constant fraction discriminator

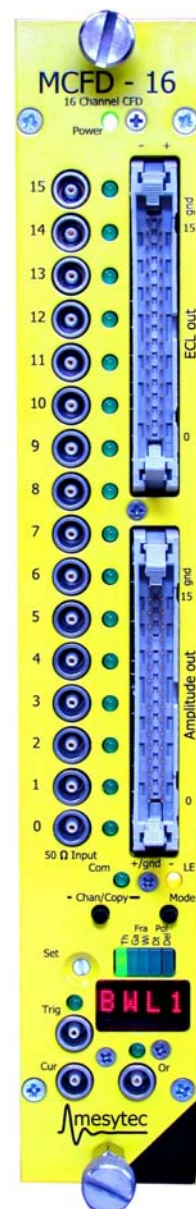
- All parameters adjustable by front panel and remote control
- Standard delay chips (SIP-7), default 20 ns
- Pulse width, dead time: 20 ns to 1.2 us
- Fraction 20% and 40%
- Delay in 5 steps (default 4 ns to 20 ns)
- Walk +-100 ps (input range 35 mV to 3.5 V)
- Lowest signal at Gain = 1 is 1.2 mV
- CFD or leading edge selectable
- 16 ECL outputs
- Common OR (NIM) and current output (1mA/chan)

### Pattern processing

- Common OR
- Multiplicity
- Full pair coincidence matrix
- Coincidence window 5 ns to 1000 ns
- Built in gate generator
- 3 NIM / TTL Trigger outputs, one veto input

### Control

- Front panel
- USB
- mesytec control bus



**Technical Data:****Fast Preamplifier**

- Inputs:  
16 Lemo signal inputs, 50 Ohm terminated.  
Amplitude range (offset + signal);  
positive -2 V to +3.5 V  
negative +2 V to -3.5 V
- Polarity:  
Input polarity configurable by front panel and RC
- Range:  
linear input range (signal only):  
Gain = 1 : 0 V to +- 3.5 V,  
Gain = 3 : 0 V to +-1.2 V,  
Gain = 10 : 0 V to +- 350m V
- Minimum detectable signal:  
(@ 25 ns rise time)

Gain	CFD-mode (100% triggers)	LE-mode (100% triggers)
1	5mV	1.2mV
3	2mV	0.8mV
10	1mV	0.5mV

- Bandwidth Limit:  
MCFD-16 has a 300 MHz bandwidth preamplifier which is limited internally to 150 MHz. This results in 2 ns rise time. When bandwidth limit is set, the bandwidth is reduced to 30 MHz, which results in 10 ns rise time

**Discriminator**

- Threshold

Gain	Range (set value 0...255)
1	max 100 mV
3	max 30 mV
10	max 10 mV

- Width and dead time adjust

Width and dead time can be adjusted in the range of 20ns to 1.2us  
Dead time is the time from pulse start to the next possible pulse.

- Automatic offset compensation (Auto walk):

Works for all signals with signal + offset within specified amplitude range.

Walk (25 ns risetime signal) Gain = 1, Amplitude 35m V to 3.5 V: +- 100 ps

- Delay

Configurable via front panel or RC: 5 taps with 4 ns each (with SIP-7 standard delay chips, 20 ns, 100 R). Standard delay chips from all manufacturers can be used.

Fraction settable via front panel or RC: 20 % and 40 %.

CFD Crosstalk < 60 dB (1000:1) for all types of signals within allowed input range.  
No neighbour channel triggers under any conditions.

Delays:

CFD zero crossing takes place at the pulse maximum, so timing is referenced to the pulse maximum.

Output	Delay[ns]
individual ECL outputs	2 ns
Fast OR output	10 ns
Trig 0, 1, 2	typ 25 ns

**Channel mask**

Inputs can be masked individually using RC control. A "1" in the mask string deactivates corresponding channel.

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**Timing Outputs**

- 16 ECL discriminator outputs
- 1x current OR output, 1mA per hit
- 1x fast logic OR output NIM, delay 10 ns from pulse maximum

**Analog output:**

Signal after amplification 1, 3 or 10.  
Can be jumper configured as unipolar or differential signal.  
Max  $\pm 3.5$  V unterminated.  
Source resistance 50 Ohm (2x50 Ohm differential)

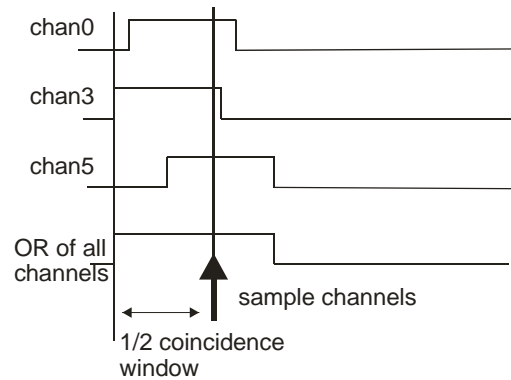
**Data interfaces**

- USB 2.0 connector
- mesytec control bus (Lemo "00" and ID-coder)

**Coincidence unit, counters, digital processing****Coincidence time**

MCFD-16 provides two different types of coincidences:

- **Fast precision coincidence:**  
Is a latched coincidence. A logic OR of all inputs starts a delay generator. After delay runs out the signals are sampled simultaneously, and the pattern is evaluated. The delay can be as short as 2.5ns, resulting in a coincidence time of 5ns.  
Coincidence window is as short as 5 ns and goes up to 1000 ns. The output pulse width is fixed 60 ns and is generated about 25 ns after the input pulse maximum.



- **Overlap coincidence:**  
Simple overlap coincidence. The window is 2 times the width of the channel output pulses. Its range is from 40 ns to 2.4  $\mu$ s. The output pulse width at trigger outputs is determined by the overlap time of the input signals.

**Gate generator:**

The built in gate generator can be used to generate an output pulse with adjustable rising and falling edge. Minimum delay (from trigger generation) is 10 ns, maximum is 1 us.

Any of the three pattern sources can trigger the GG.

- 3x Trigger outputs, configurable TTL or NIM. Pulse length typ. 60ns.
- Configurable sources:
- OR
  - Multiplicity
  - full Pair coincidence matrix
  - internal gate generator 10 ns to 1 us.

**Power consumption:****Veto input:**

Can be configured to Veto the trigger outputs.

Input signal, dual level: NIM or TTL.

+12V	100 mA
+6V	1.2 A
-6V	2.0 A

Total power consumption:

Gain = 1: max 16 W

Gain = 10: max 20 W

**Trigger outputs:****How to set the configuration**

Value which can only be set by a switche on the mother board:

output level for trigger 0 (front panel) and trigger 1 and 2 (rear side). The level can be switched from NIM (default) to TTL. The switch is near the front panel on the mother board.

The parameters “Leading Edge” and “bandwidth limit” can be set by two switches on the mother board.

(near the rear panel) and is valid for all channels. The value can be changed by remote control when the “RC” flag is on. (type “ON” at USB connection, then BWL 1/0 and CFD1/0).

The seven main parameters: **threshold, gain, width, dead time, delay, fraction and polarity** can be set via front panel, USB, and in the next firmware revision by control bus.

Thresholds can be set individually for the channels.

The other parameters are always common to two channels. The pairs are 0/1, 2/3,...14/15.

So  $16 + 6 \times 8 = 64$  values can be set to define the module operation.

To make the setting easier a common mode is implemented. When switched on, the channel values are set to the same value for all channels. Then only the 7 parameters have to be adjusted. The common mode is set on the front panel by pressing the “chan” switch multiple times until “com” LED lights up. At USB remote control type “MC”.

For many applications with identical channels this may be an easy operation mode.

The set of common values can be copied to the individual register set by pressing the chan/copy switch for some seconds. This helps to get good start values for all channels. The individual register set gets active when “individual mode” is active. This is done by pressing the “chan” switch until “com” LED gets off. (Via USB type “MI”).

Now the individual values for each channel or channel pairs can be modified. For example polarity for channel groups may be different, or thresholds may have to be adjusted to the noise limit.

At front panel operation press the “mode” knob until the right parameter is indicated, then set the channel to be modified by the “chan” switch. When only pairs can be modified, this will be indicated by the channel LEDs.

**Pattern processing:**

MCFD-16 offers several sophisticated methods for pattern processing:

**Multiplicity detection**

An upper and lower threshold for the multiplicity can be set. A trigger is generated when:

$$\text{low\_limit} \leq \text{multiplicity} \leq \text{high\_limit}$$

For example:

- $\text{low\_limit} = 2, \text{high\_limit} = 2 \Rightarrow$  all events with multiplicity exactly = 2 create a trigger
- $\text{low\_limit} = 1, \text{high\_limit} = 4 \Rightarrow$  all events with a multiplicity between 1 and 4 create a trigger

**Coincidence matrix for Pair Coincidence Detection.**

For PET and many other applications, a pair coincidence between several detectors has to be detected to filter out correct pair events from a flood of events to be rejected.

The universal coincidence relation in such a setup can be defined by a coincidence matrix.

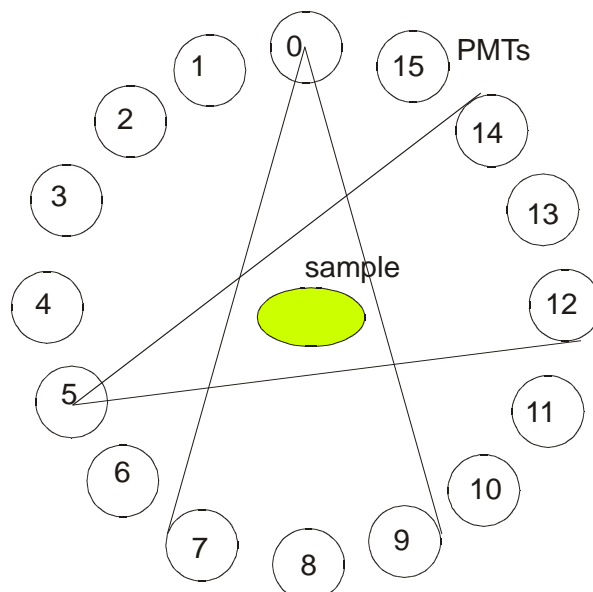
Due to the symmetry of a coincidence (1 coincident to 7 also means 7 coincident to 1) less than half of the matrix is needed for a full description of universal pair coincidences.

**Example 1: PET**

Given is a ring of PMT gamma detectors around a sample emitting positron annihilation radiation.

Search for the coincidence between one channel and any of 3 channels on the opposite side of the ring. Two of those symmetries are shown in the picture below.

When PMT 0 detects a gamma, the other one (if not scattered or lost) must be detected in PMT 7, 8 or 9 (and similar around the circle for all other PMTs) Those are the only valid events which should start the data acquisition.



The coincidences shown for the setup above can be translated to a coincidence matrix in the following way (all unoccupied fields have to be filled with "0"):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Pair coinc. register
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		1	PA1
X	X	X	X	X	X	X	X	X	X	X	X	X	X			2	PA2
X	X	X	X	X	X	X	X	X	X	X	X	X				3	PA3
X	X	X	X	X	X	X	X	X	X	X	X					4	PA4
X	X	X	X	X	X	X	X	X	X	X						5	PA5
X	X	X	X	X	X	X	X	X	X							6	PA6
X	X	X	X	X	X	X	X	X							1	7	PA7
X	X	X	X	X	X	X	X							1	1	8	PA8
X	X	X	X	X	X	X							1	1	1	9	PA9
X	X	X	X	X	X							1	1	1		10	PA10
X	X	X	X	X							1	1	1			11	PA11
X	X	X	X							1	1	1				12	PA12
X	X	X							1	1	1					13	PA13
X	X							1	1	1						14	PA14
X							1	1	1							15	PA15

Resulting in the following MCFD-16 pair coincidence pattern:

	binary	decimal
PA1 =	0	= 0
PA2 =	00	= 0
PA3 =	000	= 0
PA4 =	0000	= 0
PA5 =	0 0000	= 0
PA6 =	00 0000	= 0
PA7 =	000 0001	= 1
PA8 =	0000 0011	= 3
PA9 =	0 0000 0111	= 7
PA10 =	00 0000 1110	= 14
PA11 =	000 0001 1100	= 28
PA12 =	0000 0011 1000	= 56
PA13 =	0 0000 0111 0000	= 112
PA14 =	00 0000 1110 0000	= 224
PA15 =	000 0001 1100 0000	= 448

Coincidence should for example be accepted within a window of 10 ns.

This can only be set by remote control – here for example by a USB command (please see listing below for details on RC commands):

```
SC 25
```

The pair coincidence result should trigger Trig0 (front panel), data acquisition busy should veto this output:

```
TR 0 68 (bit 6 and 2 set)
```

Trig1 should output all events with all multiplicities (e.g. for total rate monitoring):

```
TR 1 1 // output OR of all channels
```

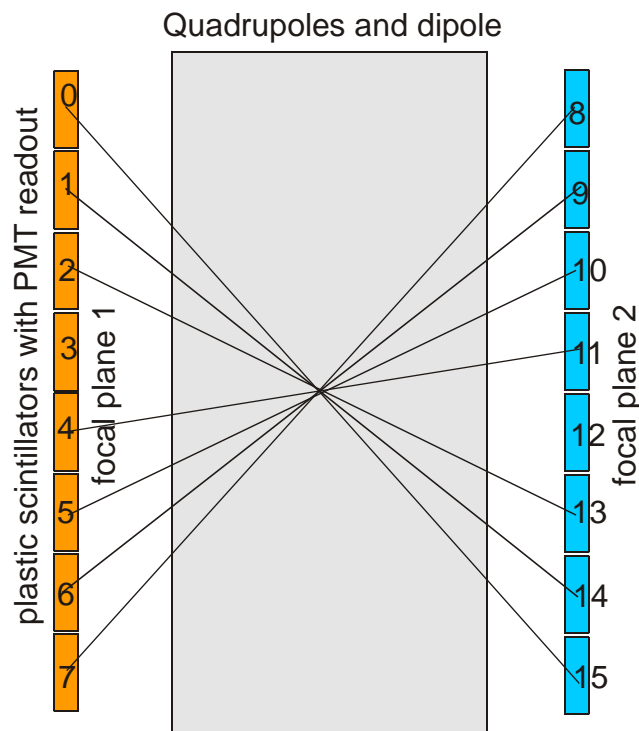
Trig2 should output events with multiplicity 2 and higher (e.g. for monitoring total coincidence rate)

```
SM 0 2 // 2 <= mult
SM 1 15 // mult <= 15
TR 2 2 // trigger on multiplicity
```

## Example 2: Fragment separator

Position and timing of particles is measured via two focal plane detectors consisting of segmented plastic scintillators. Light output is converted by a multi anode photo multiplier.

The ion optics limits the valid event tracks of a specified rigidity to the tracks shown below. A valid event triggers the data acquisition.



**resulting coincidence matrix:**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Pair coinc. register
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		1	PA1
X	X	X	X	X	X	X	X	X	X	X	X	X	X			2	PA2
X	X	X	X	X	X	X	X	X	X	X	X	X				3	PA3
X	X	X	X	X	X	X	X	X	X	X	X					4	PA4
X	X	X	X	X	X	X	X	X	X	X						5	PA5
X	X	X	X	X	X	X	X	X	X							6	PA6
X	X	X	X	X	X	X	X	X								7	PA7
X	X	X	X	X	X	X	X	1								8	PA8
X	X	X	X	X	X	X			1							9	PA9
X	X	X	X	X	X					1						10	PA10
X	X	X	X	X							1					11	PA11
X	X	X	X									1				12	PA12
X	X	X											1			13	PA13
X	X													1		14	PA14
X															1	15	PA15

## Initialise MCFD16 pair coincidence pattern:

	binary	decimal
PA1	= 0	= 0
PA2	= 00	= 0
PA3	= 000	= 0
PA4	= 0000	= 0
PA5	= 0 0000	= 0
PA6	= 00 0000	= 0
PA7	= 000 0000	= 0
PA8	= 1000 0000	= 128
PA9	= 0 0100 0000	= 64
PA10	= 00 0010 0000	= 32
PA11	= 000 0001 0000	= 16
PA12	= 0000 0000 1000	= 8
PA13	= 0 0000 0000 0100	= 4
PA14	= 00 0000 0000 0010	= 2
PA15	= 000 0000 0000 0001	= 1

## Remote control

### CMD set MCFD-16

for all channel specific commands:  
 chan = [0...16] for threshold settings  
 chan = [0...8] for all other settings  
 where chan = 16 / 8: common setting

### Preamplifier

SP chan val	chan = [0...8] val = 0/1	set polarity for channel pairs (0...7, 8 = common) to val 0 = positive, 1 = negative
SG chan val	chan = [0...8] val = 1 / 3 / 10	set gain for channel pairs (0...7, 8 = common) to val
BWL val	val = 0/1	switch Bandwidth Limit off/on

### Discriminator

CFD val	val = 0/1	switch between Leading edge (0) and Constant fraction (1)
ST chan val	chan = [0...16] val = [0...255]	set threshold for channel (0...15, 16 = common) to val
SW chan val	chan = [0...8] val = [0...255]	set width for channel pairs (0...7, 8 = common) to val → see translation table
SD chan val	chan = [0...8] val = [0...255]	set deadtime for channel pairs (0...7, 8 = common) to val → see translation table
SY chan val	chan = [0...8] val = [1...5]	set delay line (taps), channel pairs (0...7, 8 = common) to val
SF chan val	chan = [0...8] val = 20/40	set fraction for channel pairs (0...7, 8 = common) to val = 20% / 40 %
SK chan val	chan = 0/1 val = [0...255]	set masking bitmask for channels 0...7 (reg = 0) and 8...15 (reg = 1). Masked channels are deactivated.

**Pattern Processing**

SC val      val = [0, 20...255]      global coincidence time to val → see translation table.  
When set to "0" the overlap coincidence gets active

TR n val      n=0,1,2      set trigger source for front (0), rear1 (1), rear2 (2) trigger  
val = [0...255]      possible sources:

Bit 7 (128)	Bit 6 (64)	Bit 5	Bit 4	Bit 3	Bit 2 (4)	Bit 1 (2)	Bit 0 (1)
GateGen.	Veto	0	0	0	Pair Coinc.	Multiplic.	OR

When "Veto" bit is activated, the output can be inhibited by the Veto input (Rear side Lemo).

GS val      val = [0...7]      set source for gate generator:

Bit 2 (4)	Bit 1 (2)	Bit 0 (1)
Pair Coinc.	Multiplic.	OR

GA n val      n = 0/1      set gate timing. n=0: leading edge, n=1: trailing edge  
val = [0...255]      val = time [0...255] → see translation table  
required condition: GA 1 > GA 0

SM n val      n = 0/1      set thresholds for multiplicity trigger: n=0: lower value  
val = [0...15]      n=1: upper value. Condition: lower < upper

PA n val      n = [1...15]      set pattern for pair coincidence  
val = ...

DP      display pair coincidence table

**Test function**

Pn            n = 0/1            switch builtin testpulser off / on. Injects 50mV pulses with risetime 2ns, decay time 50ns.

**Special commands**

Mx            x=I, C            switch mode to Individual / Common

ON            switch RC on (RC defined BWL and CFD settings dominate over hardware settings)

OFF            switch RC off (BWL and CFD settings are defined by hardware settings)

GR chan            get event rate in given channel (0...15)  
16..18 = trig0..2, 19 = total rate

DS            display all the setup

V            display firmware version

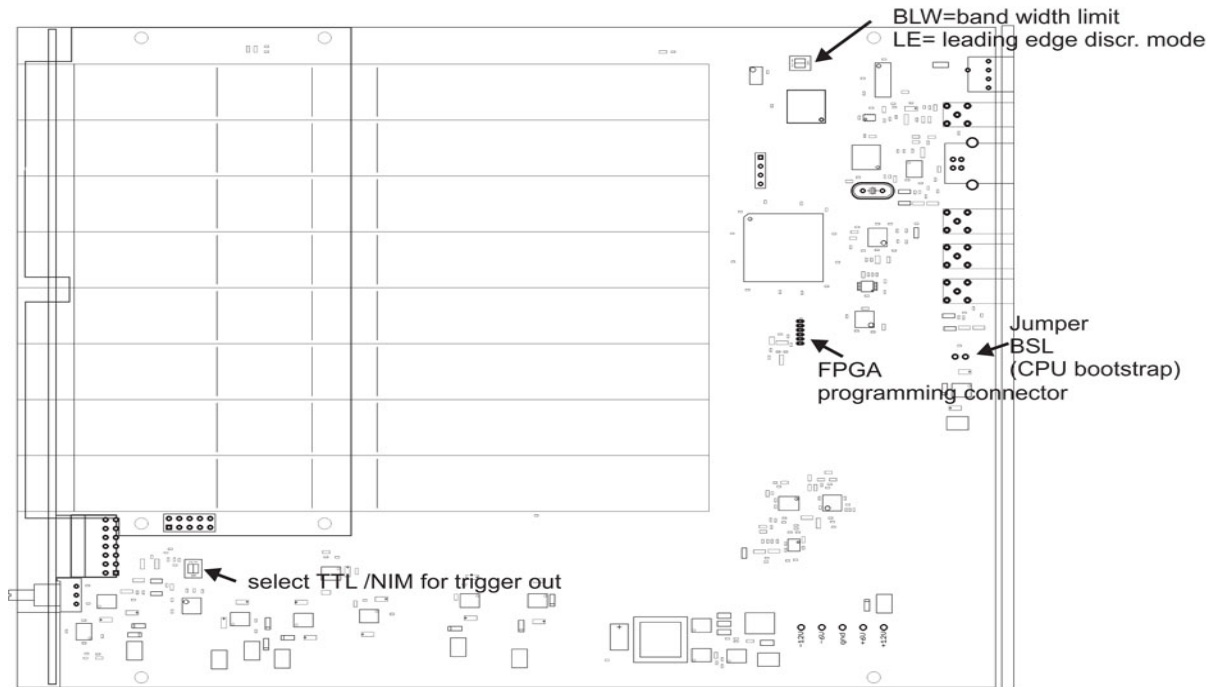
?            display command summary

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**Not implemented in the present test revision:**

- 1) mesytec control bus
- 2) a lot of resources are still available for further coincidence conditions
- 3) counters can be implemented for special purpose.

Overview, elements inside the box



**Conversion tables**

the real time values values are also shown at the front panel and as USB input response.

