MCFD-16

(Data sheet V1.8_13)

16 channel CFD
with fast amplifier
and pattern processing

mesytec **MCFD-16** is an easy to use, fast 16 channel constant fraction discriminator (CFD) for high timing resolution applications. It provides fast amplifiers at the inputs which can be set for input polarity and gains. The amplifier outputs are split to the CFD unit and are available as unipolar or differential signals (configurable) at an output connector. The discriminator signals are available as ECL differential outputs at a 34 pin header connector.
In differential mode, the analogue outputs allow to drive long twisted pair delay cables to introduce the necessary delay needed for charge sensitive ADCs (QDCs).
A fast pattern processing is implemented, well suited to produce complex triggers from input coincidences. An optimised type (MCFD-16-fast) for signal rise times below 2 ns is available.

Features:

Built in fast pre amplifier
- Gain 1, 3, and 10
- Polarity selectable
- 300MHz band width
- Analog Output: configurable via Jumper: unipolar or differential

Constant fraction discriminator
- All parameters adjustable by front panel and remote control
- Standard delay chips (SIP-7, 100 Ω), default 20 ns
- Pulse width: 6 ns to 660 ns, dead time 20 ns to 660 ns
- Fraction 20 % and 40 %
- Delay in 5 steps (default 4 ns to 20 ns)
- Walk ±100 ps (input range 35 mV to 3.5 V)
- Lowest signal for 100 % trigger at gain = 1 is 2 mV
- CFD or leading edge discrimination selectable
- 16 ECL* outputs
- Common OR (NIM) and current output (0.5 mA/chan)

Pattern processing
- Common OR
- Or of two independent definable groups of channels
- Multiplicity
- Full pair coincidence matrix
- Coincidence window 5 ns to 600 ns
- Built in gate generator
- 3 NIM / TTL trigger outputs, one veto input

Control
- Front panel, USB, mesytec control bus

Output Options*: ECL (standard),
LVDS, NIM (has no splitted analog output !)

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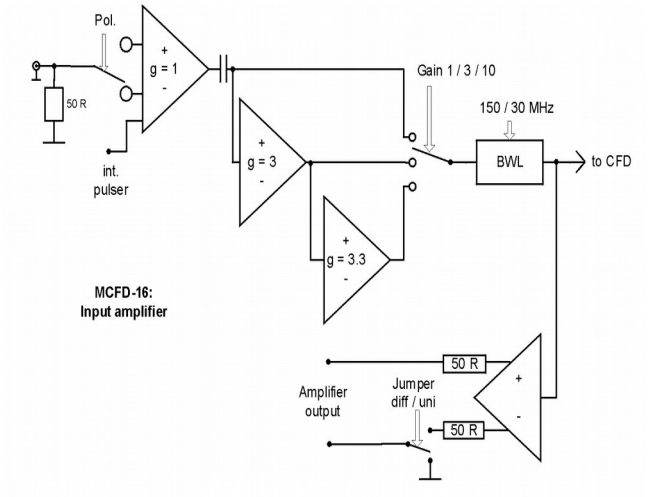
Technical Data

Fast Pre amplifier

The built in fast amplifiers can be set to a gain of 1, 3, and 10.
The polarity can be selected positive and negative. The outputs are available differential or unipolar at a 34 pin header connector at the front panel. In differential output configuration, the signals can be delayed via twisted pair cable, and can directly be fed to QDC
inputs. The -3 dB bandwidth of the amplifiers is 600 MHz, 500 MHz and 300 MHz for gain 1, 3 and 10. The high bandwidth is important to minimise the influence of amplitude on the pulse shape due to non linear effects in the amplifiers. After the amplifier the bandwidth is limited to 150 MHz by a filter, to reduce the noise band width, but preserve rise times down to 2 ns. Optional a filter with a cut off at 30 MHz can be introduced to further reduce noise for signals with rise times below 10 ns.
The input signals are AC-coupled with a time constant of 150 us. This allows a wide range of offsets at the input without affecting the CFD. The baseline shift introduced by AC-coupling at extreme rates, is compensated in the CFD by automatic offset adjust.



Gain, polarity and band width can be set by front panel or via remote control.

Short data

- Inputs:
  16 Lemo inputs, 50 Ω terminated.
  Amplitude range (offset + signal);
  Positive –2 V to +3.5 V
  Negative +2 V to –3.5 V

- Polarity:
  Input polarity configurable by front panel and RC

- Range:
  linear input range (signal only):
  Gain = 1 : 0 V to ±3.5 V,
  Gain = 3 : 0 V to ±1.2 V,
  Gain = 10 : 0 V to ±350 mV

- Minimum detectable signal:
  (@ 25 ns rise time)

Gain	CFD-mode (100% triggers)	LE-mode (100% triggers)
1	3 mV	2 mV
3	1.5 mV	1 mV
10	1 mV	0.5 mV

- Bandwidth Limit:
  MCFD-16 has a 600 to 300 MHz bandwidth (depending on gain) pre amplifier which is limited internally to 150 MHz. This results in 2 ns rise time.
  When bandwidth limit is set, the bandwidth is reduced to 30 MHz, which results in 10 ns rise time

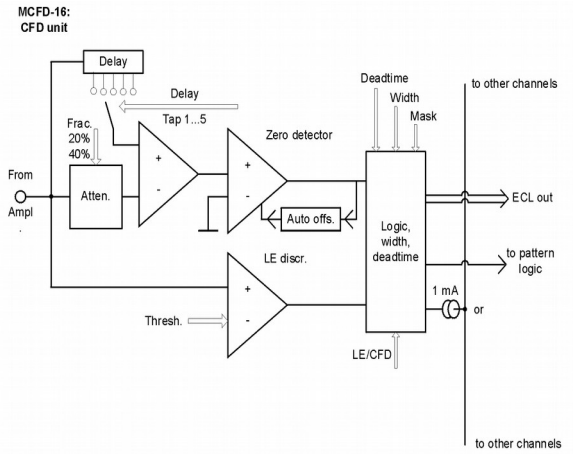
Discriminator

The constant fraction discriminator consists of a leading edge discriminator and a zero crossing discriminator.
The input signal is attenuated and inversely added to the delayed input signal. The zero crossing of this signal is independent of the signal amplitude. So compared to a simple leading edge discriminator the time walk with amplitude is eliminated.
For MCFD-16, the fraction (attenuation) can be electronically selected to 20 % or 40 %.
The delay is created by a standard delay chip (SIP7, impedance 100 Ω) with 5 taps. The delay can be selected electronically. It is set to be the time between the fraction point and the maximum of the pulse.

The offset of the zero crossing detector is automatically set, and so cancels baseline shift and low frequency noise. The zero crossing discriminator can be switched off, so only the leading edge discriminator stays active (LE-mode).
MCFD-16 is designed for lowest noise and cross talk, and allows to operate the CFD with a dynamic range of 1000:1 (3.5 V to 3 mV).
In LE-discriminator mode it provides a dynamic range of 1750:1 (3.5 V to 2 mV).

The CFD provides a walk of only +/-100 ps for pulse rise times of 25 ns and a dynamic range of 100:1.

The 16 channels of discriminator provide 16 ECL differential output signals at the front panel with a delay of 2 ns from pulse maximum. A fast common “OR” signal (delay 10 ns from pulse maximum) is created when any of the channels responds. Also a current signal with 0.5 mA per responding channel is available.



Short data

- Threshold

Gain	Range (set value 0...255)
1	max 250 mV
3	max 75 mV
10	max 25 mV

- Timing resolution (Sigma, single channel)

MCFD16_V18 standard type

Amplitude	@ rise time = 20 ns	@ rise time = 2 ns
0.1 V	60 ps	25 ps
0.5 V	19 ps	7 ps
2 V	6 ps*	5 ps*

MCFD16_V18 fast type

Amplitude	@ rise time = 0.5 ns	@ rise time = 2 ns
0.05 V	22 ps	
0.1 V	12 ps	18 ps
0.5 V	5 ps*	6 ps*
2 V		5 ps*

* Limit of measurement equipment

- Width and dead time adjust
  Width can be adjusted in the range of 6 ns to 660 ns.
  (Note, coincidence unit can only work when width > coincidence time !)
  Dead time is the time from pulse end to the next possible pulse. Dead time is 20 ns to 660 ns.

- Automatic offset compensation (Auto walk):
  Works for all signals with signal + offset within specified amplitude range.

- Walk (25 ns rise time signal) Gain = 1, Amplitude 35 mV to 3.5 V: ±100 ps

- Delay configurable via front panel or RC: 5 taps with 4 ns each (with SIP-7 standard delay chips, 20 ns, 100 Ω). Standard delay chips from all manufacturers can be used. Delay chips from 5 ns to 100 ns are available.

- Fraction settable via front panel or RC: 20 % and 40 %.

- CFD Crosstalk < 60 dB (1000:1) for all types of signals within allowed input range. Input related cross talk < 1 mV.

- Output delays:
  CFD zero crossing takes place at the pulse maximum, so timing is referenced to the pulse maximum.

Output	Delay[ns]
individual ECL outputs	2 ns
Fast OR output	10 ns
Trig 0, 1, 2	Typ. 25 ns

Channel mask

Inputs can be masked in pairs, using RC control. A "1" in the mask string deactivates corresponding channel pair.

Timing Outputs

- 16 ECL discriminator outputs
- 1x current OR output, 0.5 mA per hit
- 1x fast logic OR output NIM, delay 10 ns from pulse maximum

Analogue output

- Signal after amplification 1, 3 or 10.
- Can be jumper configured as unipolar or differential signal.
- Max ±3.5 V unterminated.
- Source resistance 50 Ω
  (2x 50 Ω differential)

Data interfaces

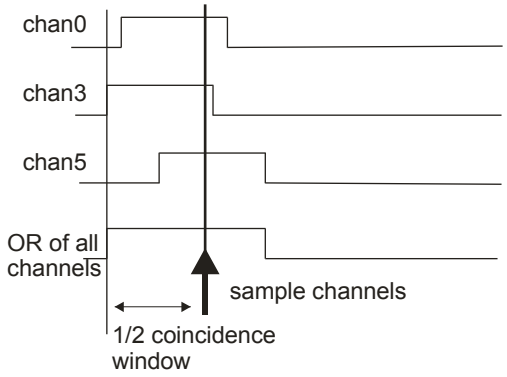
- USB 2.0 connector
- mesytec control bus (Lemo ”00” and ID-coder

Coincidence unit, counters, digital processing

Coincidence time

MCFD-16 provides two different types of coincidences:

- Fast precision coincidence:
  Is a latched coincidence. A logic OR of all inputs starts a delay generator. After delay runs out the signals are sampled simulta neously, and the pattern is evaluated. The delay can be as short as 2.5 ns, resulting in a coincidence time of 5 ns. Coincidence window is as short as 5 ns and goes up to 1000 ns.
  The coincidence only works properly when the discriminator pulse width is larger or equal the coincidence window !



  The trigger output pulse width is fixed 60 ns and is generated about 25 ns after the coincidence is detected (sample time).

- Overlap coincidence:
  Simple overlap coincidence. The window is 2 times the width of the channel output pulses. So its range is from 12 ns to 1.3 us.
  The output pulse width at trigger outputs is determined by the overlap time of the input signals.

Gate generator

The built in gate generator can be used to generate an output pulse with adjustable delay for rising and falling edge.
Minimum delay (from trigger generation) is 10 ns, maximum is 1 us. Any of the three pattern sources can trigger the GG.

Veto input

Can be configured to Veto the trigger outputs.
Input signal: dual level: NIM or TTL.

Trigger outputs

- 3x Trigger outputs, configurable TTL or NIM.
  Pulse length typ. 60 ns.
  Configurable sources:
  - OR (any list of channels definable)
  - Multiplicity
  - full Pair coincidence matrix
  - internal gate generator 10 ns to 1 us.

Power consumption (max)

+12 V:	20 mA
+6 V:	1.4 A
–6 V:	2.2 A

- Total power consumption:
  Gain = 1: max 17 W
  Gain = 10: max 22 W

How to set the configuration

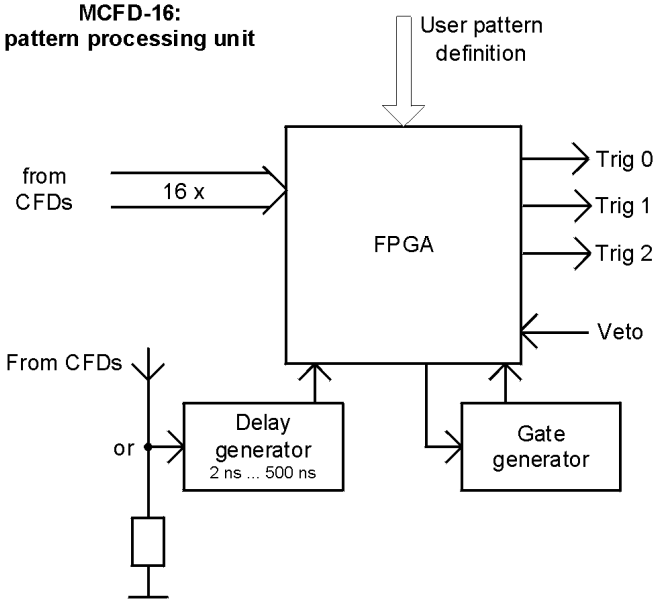
Value which can only be set by a switch on the mother board:
output level for trigger 0 (front panel) and trigger 1 and 2 (rear side). The level can be switched from NIM (default) to TTL. The switch is near the front panel on the main board.

The parameters “Leading Edge” and “Band Width Limit” can be set by two switches on the main board. (near the rear panel) and are valid for all channels. The value can be changed by remote control when the “RC” flag is on. (type “ON” at USB connection, then set BWL 1/0 and CFD1/0).

The seven main parameters: **threshold, gain, width, dead time, delay, fraction and polarity** can be set via front panel, USB, and by mesytec control bus.
Thresholds can be set individually for the channels.
The other parameters are always common to two channels. The pairs are 0/1, 2/3,...14/15.
So 16 + 6 x 8 = 64 values can be set to define the module operation.
To make the setting easier a common mode is implemented. When common mode is active, the channel values are set to the same value for all channels. Then only the 7 parameters have to be adjusted. The common mode is set on the front panel by pressing the “chan” switch multiple times until “com” LED lights up. At USB remote control type “MC”.
For many applications with identical channels, this may be an easy operation mode.
The set of common values can be copied to the individual register set by pressing the chan/copy switch for some seconds. This helps to get good start values for all channels. The individual register set gets active when “individual mode” is active. This is done by pressing the “chan” switch, then “com” LED gets off. (Via USB type “MI”).
Now the individual values for each channel or channel pairs can be modified. For example polarity for channel groups may be different, or thresholds may have to be adjusted to the noise limit.
At front panel operation press the “mode” knob until the right parameter is indicated, then set the channel to be modified by the “chan” switch. When only pairs can be modified, this will be indicated by the channel LEDs.

Pattern processing

MCFD-16 offers several sophisticated methods for pattern processing:



Multiplicity detection

An upper and lower threshold for the multiplicity (number of responding channels) can be set.
A trigger is generated when:

low_limit <= multiplicity <= high_limit

For example:

- low_limit = 2, high_limit = 2 => all events with multiplicity exactly = 2 create a trigger
- low_limit = 1, high_limit = 4 => all events with a multiplicity between 1 and 4 create a trigger

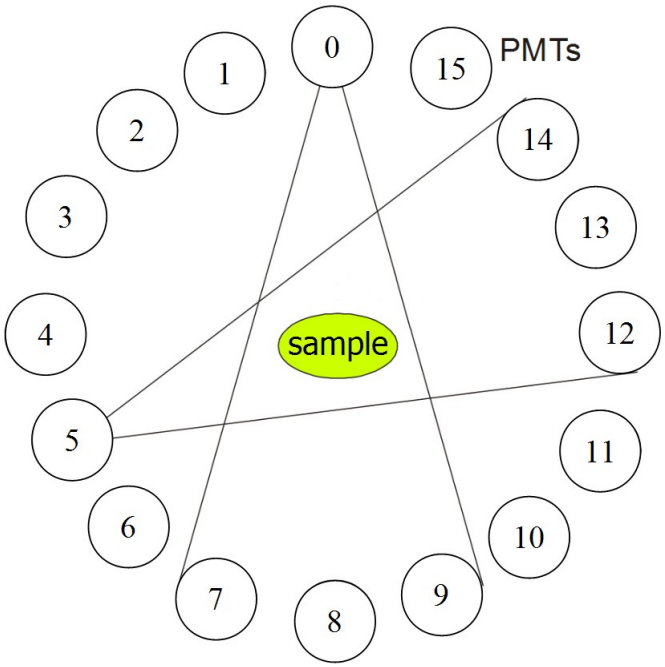
Coincidence matrix for Pair Coincidence Detection

For PET and many other applications, a pair coincidence between several detectors has to be detected to filter out correct pair events from a flood of events to be rejected.

The universal coincidence relation in such a setup can be defined by a coincidence matrix.
Due to the symmetry of a coincidence (1 coincident to 7 also means 7 coincident to 1) less then half of the matrix is needed for a full description of universal pair coincidences.

Example 1: PET

Given is a ring of PMT gamma detectors around a sample emitting positron annihilation radiation.
Search for the coincidence between one channel and any of 3 channels on the opposite side of the ring.
Two of those symmetries are shown in the picture below.
When PMT 0 detects a gamma, the other one (if not scattered or lost) must be detected in PMT 7, 8 or 9 (and similar around the circle for all other PMTs) Those are the only valid events which should start the data acquisition.



The coincidences shown for the setup above can be translated to a coincidence matrix in the following way (all unoccupied fields have to be filled with "0"):

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Pair coinc. register
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		1	PA1
X	X	X	X	X	X	X	X	X	X	X	X	X	X			2	PA2
X	X	X	X	X	X	X	X	X	X	X	X	X				3	PA3
X	X	X	X	X	X	X	X	X	X	X	X					4	PA4
X	X	X	X	X	X	X	X	X	X	X						5	PA5
X	X	X	X	X	X	X	X	X	X							6	PA6
X	X	X	X	X	X	X	X	X							1	7	PA7
X	X	X	X	X	X	X	X							1	1	8	PA8
X	X	X	X	X	X	X							1	1	1	9	PA9
X	X	X	X	X	X							1	1	1		10	PA10
X	X	X	X	X							1	1	1			11	PA11
X	X	X	X							1	1	1				12	PA12
X	X	X							1	1	1					13	PA13
X	X							1	1	1						14	PA14
X							1	1	1							15	PA15

Resulting in the following MCFD-16 pair coincidence pattern:

		binary	decimal
PA1	=	0	= 0
PA2	=	00	= 0
PA3	=	000	= 0
PA4	=	0000	= 0
PA5	=	0 0000	= 0
PA6	=	00 0000	= 0
PA7	=	000 0001	= 1
PA8	=	0000 0011	= 3
PA9	=	0 0000 0111	= 7
PA10	=	00 0000 1110	= 14
PA11	=	000 0001 1100	= 28
PA12	=	0000 0011 1000	= 56
PA13	=	0 0000 0111 0000	= 112
PA14	=	00 0000 1110 0000	= 224
PA15	=	000 0001 1100 0000	= 448

Coincidence should for example be accepted within a window of 10 ns.
This can only be set by remote control – here for example by a USB command
(please see listing below for details on RC commands):

SC 17 (set coincidence to 10 ns)
SW 8 45 (set width of outputs to 50 ns,
must be more than coincidence time of 10 ns !!)

The pair coincidence result should trigger Trig0 (front panel), data acquisition busy should veto this output:

TR 0 68 (bit 6 = veto and bit 2 = pair coincidence are set)

Trig1 should output all events with all multiplicities (e.g. for total rate monitoring):

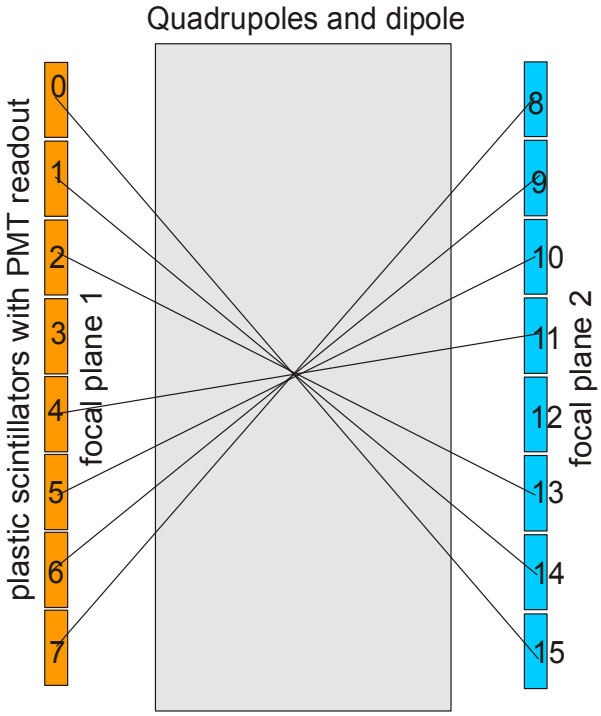
TR 1 1 (bit 0 = output OR of all channels)

Trig2 should output events with multiplicity = 1

SM 1 1 (mult = 1)
TR 2 2 (bit 1 = trigger on multiplicity)

Example 2: Fragment separator

Position and timing of particles is measured via two focal plane detectors consisting of segmented plastic scintillators. Light output is converted by a multi anode photo multiplier.
The ion optics limits the valid event tracks of a specified rigidity to the tracks shown below.
A valid event triggers the data acquisition.



resulting coincidence matrix:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Pair coinc. register
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		1	PA1
X	X	X	X	X	X	X	X	X	X	X	X	X	X			2	PA2
X	X	X	X	X	X	X	X	X	X	X	X	X				3	PA3
X	X	X	X	X	X	X	X	X	X	X	X					4	PA4
X	X	X	X	X	X	X	X	X	X	X						5	PA5
X	X	X	X	X	X	X	X	X	X							6	PA6
X	X	X	X	X	X	X	X	X								7	PA7
X	X	X	X	X	X	X	X	1								8	PA8
X	X	X	X	X	X	X			1							9	PA9
X	X	X	X	X	X					1						10	PA10
X	X	X	X	X							1					11	PA11
X	X	X	X									1				12	PA12
X	X	X											1			13	PA13
X	X													1		14	PA14
X															1	15	PA15

Initialise MCFD-16 pair coincidence pattern:

	binary		decimal
PA1	=	0	= 0
PA2	=	00	= 0
PA3	=	000	= 0
PA4	=	0000	= 0
PA5	=	0 0000	= 0
PA6	=	00 0000	= 0
PA7	=	000 0000	= 0
PA8	=	1000 0000	= 128
PA9	=	0 0100 0000	= 64
PA10	=	00 0010 0000	= 32
PA11	=	000 0001 0000	= 16
PA12	=	0000 0000 1000	= 8
PA13	=	0 0000 0000 0100	= 4
PA14	=	00 0000 0000 0010	= 2
PA15	=	000 0000 0000 0001	= 1

USB-Remote control

CMD set MCFD-16

for all channel specific commands:
chan = [0...16] for threshold settings
chan = [0...8] for all other settings
where chan = 16 / 8: common setting

Preamplifier

SP pair val	pair = [0...8] val = 0/1	set polarity for channel pairs (0...7, 8 = common) to val 0 = positive, 1 = negative
SG pair val	pair = [0...8] val = 1 / 3 / 10	set gain for channel pairs (0...7, 8 = common) to val
BWL val	val = 0/1	switch Bandwidth Limit off/on (overrides hardware setting only if RC = on)

Discriminator

CFD val	val = 0/1	switch between Leading edge (0) and Constant fraction (1) (overrides hardware setting only if RC = on)
ST chan val	chan = [0...16] val = [0...255]	set threshold for channel (0...15, 16 = common) to val
SW pair val	pair = [0...8] val = [16...222]	set width for channel pairs (0...7, 8 = common) to val → see translation table
SD pair val	pair = [0...8] val = [27...222]	set dead time for channel pairs (0...7, 8 = common) to val → see translation table

SY pair val	pair = [0...8] val = [1...5]	set delay line (taps), channel pairs (0...7, 8 = common) to val
SF pair val	pair = [0...8] val = 20/40	set fraction for channel pairs (0...7, 8 = common) to val = 20 % / 40 %
SK val	val = [0...255]	set masking bit mask for channel pairs. Masked channel pairs are deactivated. Mask register:

Bit (Val)	7 (128)	6 (64)	5 (32)	4 (16)	3 (8)	2 (4)	1 (2)	0 (1)
Channels	15 + 14	13 + 12	11 + 10	9 + 8	7 + 6	5 + 4	3 + 2	1 + 0

Trigger settings / Pattern Processing

SC val	val = [0, 3...136]	global coincidence time to val → see translation table. When set to "0" the overlap coincidence gets active. (Note, width must be adjusted to more than the coinc. time)
TR n val	n=0,1,2 val = [0...255]	set trigger source for front (0), rear1 (1), rear2 (2) trigger bit field, possible sources:

Bit 7 (128)	Bit 6 (64)	Bit 5 (32)	Bit 4 (16)	Bit 3 (8)	Bit 2 (4)	Bit 1 (2)	Bit 0 (1)
GateGen.	Veto	Pat_Or_0	Pat_Or_1	Mon see **	Pair Coinc.	Multiplic.	OR
Corresponding settings (commands):							
GA, GS	-	TP	TP	TM	PA	SM	-

All selected trigger sources for a trigger output (except "veto") are ored.

Triggering options

- Gate Generator: set gate timing with "GA" and gate generator source with "GS"
- When "Veto" bit is set, the trigger output can be inhibited by the Veto input (rear side Lemo input)
- Define Ored Trigger Patterns 0 and 1 with TP
- ** For front trigger and rear1 trigger, this bit selects monitor 0 as source, for rear 2 trigger it selects monitor1. Please see command "TM" for assignment of signal channel to monitor
- Two trigger pattern (free OR selection out of the 16 signal channels) can be defined with the command "TP"
- Pair coincidence patterns are defined with command "PA"
- Multiplicity boundaries are set with "SM"

TM n chan	n = 0, 1	assign signal channel *chan* to trigger monitor *n* monitor *n* can then be selected as trigger source with the above describe command “TR”
TP n val	n = 0, 1, 2, 3 val = [0...255]	define a trigger pattern with: n = 0: low byte pattern 0 n = 1: high byte pattern 0 n = 2: low byte pattern 1 n = 3: high byte pattern 1 Bits 0...15 in trigger pattern correspond to signal channels 0...15. If any of the selected channels is triggering, a trigger signal will be generated if Pat_Or_0 or Pat_Or_1 have been selected with command TR describe above.
SV n	n = 0, 1	enable (n=1) or disable (n=0) fast veto input
GS val	val = [0...7]	set source for gate generator

Bit 7 (128)	Bit 6 (64)	Bit 5 (32)	Bit 4 (16)	Bit 3 (8)	Bit 2 (4)	Bit 1 (2)	Bit 0 (1)
-	Veto	Pat_Or_1	Pat_Or_0	Mon0 / Mon1	Pair Coinc.	Multiplic.	OR
Corresponding settings (commands):							
-	-	TP	TP	TM	PA	SM	-

GA n val — n = 0/1, val = [5...255] — set gate timing. n = 0: leading edge, n = 1: trailing edge. val = time [5...255] → see translation table. required condition: GA 1 > GA 0

SM lower upper — lower, upper = [1...16] — lower multiplicity limit, upper multiplicity limit

DT — display trigger settings

Pair Coincidence Triggering

PA n val — n = [1...15], val = … — set pattern for pair coincidence

DP — display pair coincidence table

Test function

Pn — n = 0/1/2/3 — switch built in test pulser off = 0, 2.5 MHz = 1, 1.22 kHz = 2, 3 = pos edge (TTL) or negative edge(NIM) from Veto input creates pulse. Injects 50 mV pulses with rise time 2 ns, decay time 50 ns.

Special commands

Mx — x=I, C — switch mode to Individual / Common

ON — switch RC on (RC defined BWL and CFD settings dominate over hardware settings)

OFF — switch RC off (BWL and CFD settings are defined by hardware settings)

RA chan — get event rate in given channel (0...15). chan = 16, 17, 18: trig0, trig1, trig2. chan = 19: total rate

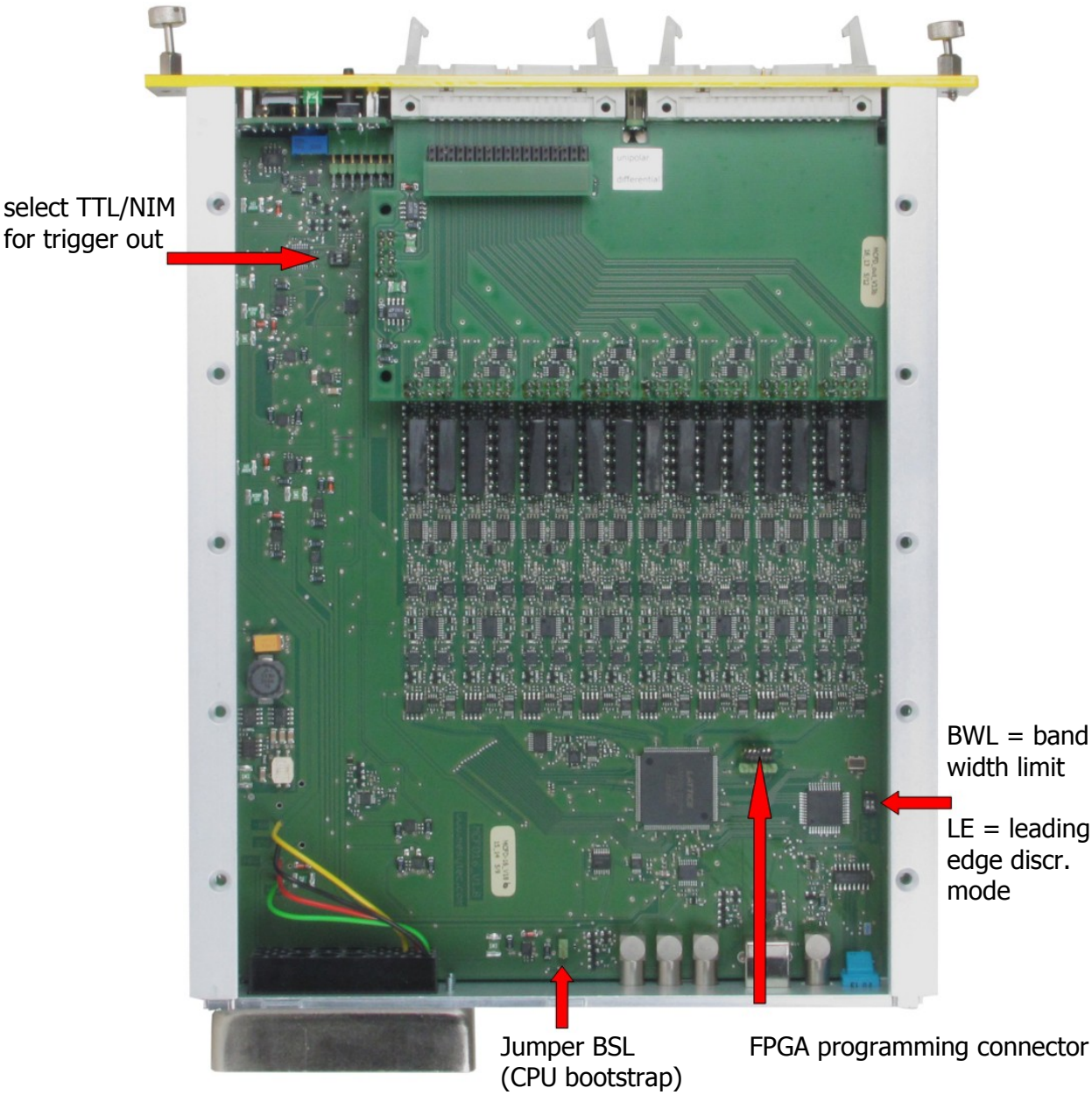
DS — display setup

V — display firmware version

? — display command summary

H

Overview, elements inside the box



Conversion tables

the real time values are shown at the front panel and as USB input response.

Width: allowed numerical values: 16 … 222 (= 6 … 664 ns)

val	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
t[ns]	6	6	6	6	9	10	12	13	15	17	18	20	21	23	25	26
val	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
t[ns]	28	30	31	33	35	36	38	40	41	43	45	46	48	50	52	53
val	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**
t[ns]	55	57	59	61	62	64	66	68	70	71	73	75	77	79	81	83
val	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**77**	**78**	**79**
t[ns]	85	87	88	90	92	94	96	98	100	102	104	106	108	110	112	114
val	**80**	**81**	**82**	**83**	**84**	**85**	**86**	**87**	**88**	**89**	**90**	**91**	**92**	**93**	**94**	**95**
t[ns]	116	118	121	123	125	127	129	131	133	135	138	140	142	144	146	149
val	**96**	**97**	**98**	**99**	**100**	**101**	**102**	**103**	**104**	**105**	**106**	**107**	**108**	**109**	**110**	**111**
t[ns]	151	153	156	158	160	162	165	167	170	172	174	177	179	182	184	186
val	**112**	**113**	**114**	**115**	**116**	**117**	**118**	**119**	**120**	**121**	**122**	**123**	**124**	**125**	**126**	**127**
t[ns]	189	191	194	197	199	202	204	207	209	212	215	217	220	223	226	228
val	**128**	**129**	**130**	**131**	**132**	**133**	**134**	**135**	**136**	**137**	**138**	**139**	**140**	**141**	**142**	**143**
t[ns]	231	234	237	239	242	245	248	251	254	257	260	263	266	269	272	275
val	**144**	**145**	**146**	**147**	**148**	**149**	**150**	**151**	**152**	**153**	**154**	**155**	**156**	**157**	**158**	**159**
t[ns]	278	281	285	288	291	294	298	301	304	308	311	314	318	321	325	328
val	**160**	**161**	**162**	**163**	**164**	**165**	**166**	**167**	**168**	**169**	**170**	**171**	**172**	**173**	**174**	**175**
t[ns]	332	336	339	343	347	350	354	358	362	366	370	374	378	382	386	390
val	**176**	**177**	**178**	**179**	**180**	**181**	**182**	**183**	**184**	**185**	**186**	**187**	**188**	**189**	**190**	**191**
t[ns]	394	399	403	407	412	416	421	425	430	434	439	444	449	454	459	464
val	**192**	**193**	**194**	**195**	**196**	**197**	**198**	**199**	**200**	**201**	**202**	**203**	**204**	**205**	**206**	**207**
t[ns]	469	474	479	484	490	495	501	506	512	518	524	530	536	542	548	554
val	**208**	**209**	**210**	**211**	**212**	**213**	**214**	**215**	**216**	**217**	**218**	**219**	**220**	**221**	**222**	
t[ns]	561	567	574	581	587	594	602	609	616	624	632	639	647	656	664	

Dead time: allowed numerical values: 27 … 222 (= 20 … 664 ns)

val												**27**	**28**	**29**	**30**	**31**
t[ns]												20	21	23	25	26
val	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
t[ns]	28	30	31	33	35	36	38	40	41	43	45	46	48	50	52	53
val	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**
t[ns]	55	57	59	61	62	64	66	68	70	71	73	75	77	79	81	83
val	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**77**	**78**	**79**
t[ns]	85	87	88	90	92	94	96	98	100	102	104	106	108	110	112	114
val	**80**	**81**	**82**	**83**	**84**	**85**	**86**	**87**	**88**	**89**	**90**	**91**	**92**	**93**	**94**	**95**
t[ns]	116	118	121	123	125	127	129	131	133	135	138	140	142	144	146	149
val	**96**	**97**	**98**	**99**	**100**	**101**	**102**	**103**	**104**	**105**	**106**	**107**	**108**	**109**	**110**	**111**
t[ns]	151	153	156	158	160	162	165	167	170	172	174	177	179	182	184	186
val	**112**	**113**	**114**	**115**	**116**	**117**	**118**	**119**	**120**	**121**	**122**	**123**	**124**	**125**	**126**	**127**
t[ns]	189	191	194	197	199	202	204	207	209	212	215	217	220	223	226	228
val	**128**	**129**	**130**	**131**	**132**	**133**	**134**	**135**	**136**	**137**	**138**	**139**	**140**	**141**	**142**	**143**
t[ns]	231	234	237	239	242	245	248	251	254	257	260	263	266	269	272	275
val	**144**	**145**	**146**	**147**	**148**	**149**	**150**	**151**	**152**	**153**	**154**	**155**	**156**	**157**	**158**	**159**
t[ns]	278	281	285	288	291	294	298	301	304	308	311	314	318	321	325	328
val	**160**	**161**	**162**	**163**	**164**	**165**	**166**	**167**	**168**	**169**	**170**	**171**	**172**	**173**	**174**	**175**
t[ns]	332	336	339	343	347	350	354	358	362	366	370	374	378	382	386	390
val	**176**	**177**	**178**	**179**	**180**	**181**	**182**	**183**	**184**	**185**	**186**	**187**	**188**	**189**	**190**	**191**
t[ns]	394	399	403	407	412	416	421	425	430	434	439	444	449	454	459	464
val	**192**	**193**	**194**	**195**	**196**	**197**	**198**	**199**	**200**	**201**	**202**	**203**	**204**	**205**	**206**	**207**
t[ns]	469	474	479	484	490	495	501	506	512	518	524	530	536	542	548	554
val	**208**	**209**	**210**	**211**	**212**	**213**	**214**	**215**	**216**	**217**	**218**	**219**	**220**	**221**	**222**	
t[ns]	561	567	574	581	587	594	602	609	616	624	632	639	647	656	664	

Coincidence time: allowed numerical values: 0, 3 … 136 (= 4 … 611 ns)

val				**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
t[ns]				4	5	5	5	6	6	6	6	6	6	7	7	7
val	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
t[ns]	8	10	11	12	12	15	17	17	19	21	24	26	29	31	34	36
val	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
t[ns]	39	41	44	47	49	52	55	57	60	63	66	68	71	74	77	80
val	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**
t[ns]	83	86	89	89	92	95	98	101	104	108	111	114	117	121	124	127
val	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**77**	**78**	**79**
t[ns]	131	134	138	141	145	149	152	156	160	164	167	171	175	179	183	187
val	**80**	**81**	**82**	**83**	**84**	**85**	**86**	**87**	**88**	**89**	**90**	**91**	**92**	**93**	**94**	**95**
t[ns]	191	196	200	204	209	213	218	222	227	231	236	241	246	251	256	261
val	**96**	**97**	**98**	**99**	**100**	**101**	**102**	**103**	**104**	**105**	**106**	**107**	**108**	**109**	**110**	**111**
t[ns]	266	272	277	283	288	294	300	306	312	318	324	330	337	344	350	357
val	**112**	**113**	**114**	**115**	**116**	**117**	**118**	**119**	**120**	**121**	**122**	**123**	**124**	**125**	**126**	**127**
t[ns]	364	372	379	387	394	402	411	419	428	436	445	455	464	474	485	495
val	**128**	**129**	**130**	**131**	**132**	**133**	**134**	**135**	**136**							
t[ns]	506	518	529	542	554	568	581	596	611							

Gate generator: allowed numerical values: 5 … 255 (= 20 … 962 ns)

val						*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*
t[ns]						20	20	20	20	21	22	23	24	26	27	28
val	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
t[ns]	30	31	32	34	35	36	37	39	40	42	43	44	46	47	48	50
val	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
t[ns]	51	52	54	55	57	58	59	61	62	64	65	67	68	70	71	73
val	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**
t[ns]	74	76	77	79	80	82	83	85	86	88	89	91	92	94	96	97
val	**64**	**65**	**66**	**67**	**68**	**69**	**70**	**71**	**72**	**73**	**74**	**75**	**76**	**77**	**78**	**79**
t[ns]	99	100	102	104	105	107	108	110	112	113	115	117	119	120	122	124
val	**80**	**81**	**82**	**83**	**84**	**85**	**86**	**87**	**88**	**89**	**90**	**91**	**92**	**93**	**94**	**95**
t[ns]	125	127	129	131	132	134	136	138	140	141	143	145	147	149	151	153
val	**96**	**97**	**98**	**99**	**100**	**101**	**102**	**103**	**104**	**105**	**106**	**107**	**108**	**109**	**110**	**111**
t[ns]	154	156	158	160	162	164	166	168	170	172	174	176	178	180	182	184
val	**112**	**113**	**114**	**115**	**116**	**117**	**118**	**119**	**120**	**121**	**122**	**123**	**124**	**125**	**126**	**127**
t[ns]	186	188	190	193	195	197	199	201	203	206	208	210	212	215	217	219
val	**128**	**129**	**130**	**131**	**132**	**133**	**134**	**135**	**136**	**137**	**138**	**139**	**140**	**141**	**142**	**143**
t[ns]	221	224	226	229	231	233	236	238	241	243	246	248	251	253	256	258
val	**144**	**145**	**146**	**147**	**148**	**149**	**150**	**151**	**152**	**153**	**154**	**155**	**156**	**157**	**158**	**159**
t[ns]	261	264	266	269	272	274	277	280	283	285	288	291	294	297	300	303
val	**160**	**161**	**162**	**163**	**164**	**165**	**166**	**167**	**168**	**169**	**170**	**171**	**172**	**173**	**174**	**175**
t[ns]	306	309	312	315	318	321	324	327	331	334	337	340	344	347	351	354
val	**176**	**177**	**178**	**179**	**180**	**181**	**182**	**183**	**184**	**185**	**186**	**187**	**188**	**189**	**190**	**191**
t[ns]	358	361	365	368	372	376	379	383	387	391	395	399	403	407	411	415
val	**192**	**193**	**194**	**195**	**196**	**197**	**198**	**199**	**200**	**201**	**202**	**203**	**204**	**205**	**206**	**207**
t[ns]	419	423	428	432	436	441	445	450	455	460	464	469	474	479	484	490
val	**208**	**209**	**210**	**211**	**212**	**213**	**214**	**215**	**216**	**217**	**218**	**219**	**220**	**221**	**222**	**223**
t[ns]	495	500	506	511	517	523	528	534	540	547	553	559	566	572	579	586
val	**224**	**225**	**226**	**227**	**228**	**229**	**230**	**231**	**232**	**233**	**234**	**235**	**236**	**237**	**238**	**239**
t[ns]	593	600	608	615	623	631	639	648	656	665	674	683	693	703	713	723
val	**240**	**241**	**242**	**243**	**244**	**245**	**246**	**247**	**248**	**249**	**250**	**251**	**252**	**253**	**254**	**255**
t[ns]	734	745	757	769	781	794	808	822	836	852	868	885	902	921	941	962

RC-bus remote control

MCFD-16 can also be controlled using the mesytec RC bus controller modules (currently MRC-1 or MRCC).

Up to 16 modules (not only MCFD-16) can be connected on one bus, up to 32 on the two buses of the MRC-1, just using T-pieces. The last module on a bus has to be terminated with 50 Ω.

All parameters are addressed through a control register page in MCFD-16 memory, which can be read/written using the MRC-1 / MRCC communication protocol.

Basic communication protocol

Each MRC command has to follow the format described below:

CMD *bus [dev] [adr] [val]*

Data format

bus	= bus number [0...1]	(addresses one of the two available buses)
dev	= device number [0…15]	(addresses one of up to 16 device per bus)
adr	= parameter number	(addresses the register cell, see table below)
val	= [0…255]	(valid values are given at the individual register descriptions)

Mnemonic Description

SC *bus*	returns id codes for every connected device on bus: IDC = 26
ON *bus dev*	activate rc for device *dev* on bus *bus*
OFF bus dev	turn off rc for device *dev* on bus *bus*
SE *bus dev adr val*	set memory cell *adr* for device *dev* on bus *bus* to value *val*
RE *bus dev adr*	read memory cell *adr* from device *dev* on bus *bus*

Memory List MCFD-16

MCFD-16 can be controlled by reading / writing the control register page via the mesytec RC bus.

Read memory by `RE bus dev adr`
Write (set) memory by `SE bus dev adr val`

The following table defines the memory layout:

Individual settings for all channels: (used in "individual" mode)

ADR	parameter	comment
0 … 15	Threshold channel 1 … 16	Values [0 … 255]
16 … 23	Gain channel pairs 1 … 8	Values: 0 = gain 1 x, 1 = gain 3 x, 2 = gain 10 x
24 … 31	Width channel pairs 1 … 8	Values [16 … 222] → see translation table
32 … 39	Dead time channel pairs 1 … 8	Values [27 … 222] → see translation table
40 … 47	Delay channel pairs 1 … 8	Values [0 … 4] = TAP1 … TAP5
48 … 55	Fraction channel pairs 1 … 8	Values: 0 = 20 %, 1 = 40 %
56 … 63	Polarity channel pairs 1 … 8	Values: 0 = positive, 1 = negative

Common settings for all channels: (used in "common" mode)

ADR	parameter	comment
64	Threshold	Values [0 … 255]
65	Gain	Values: 0 = gain 1 x, 1 = gain 3 x, 2 = gain 10 x
66	Width	Values [16 … 222] → see translation table
67	Dead time	Values [27 … 222] → see translation table
68	Delay	Values [0 … 4] = TAP1 … TAP5
69	Fraction	Values: 0 = 20 %, 1 = 40 %
70	Polarity	Values: 0 = positive, 1 = negative

Hardware settings, Mode and RC

ADR	parameter	comment
71*	Bandwidth Limit	Values: 0 = off, 1 = on. Overrides hardware switch only when RC is on
72	Mode	Values: 0 = common mode, 1 = individual mode
73	RC on/off	Values: 0 = off, 1 = on
85*	Discrimination	Values: 0 = Leading Edge, 1 = Constant Fraction Overrides hardware switch only when RC is on

*: Parameters 71 and 85 only from firmware version 2.18 upwards!

Timing parameters

ADR	parameter	comment
74	Gate Generator leading edge delay	Values [5...255] → see translation table condition: leading edge < trailing edge (will be checked and modified if set erroneously)
75	Gate Generator trailing edge delay	Values [5...255] and trailing edge > leading edge (will be checked and modified if set erroneously)
76	Coincidence time	Values [0, 3...136] → see translation table, 0 = off → overlap coincidence active
77	fast_veto	1 = directly veto the input discriminatiors with veto input

Rate measurement

78	Rate monitor channel	Values [0...19]: channel used for rate measurement 0...15: signal channels, 16...18: trig 0...2, 19: total rate
79	Time base	Values [0...15] 15 → 1 s, 7 → 1/2 s, 3 → 1/4 s, 0 → 1/8 s
80	Measurement ready (Read only)	'1' when measurement is ready.
81	Frequency * low byte (Read only)	
82	Frequency * high byte	write to this register starts new measurement

* 0xFFFF is a reserved word, and signals "data not ready". When valid data is read, the measurement is restarted after reading the high byte (register 82).

Channel mask:

83	Mask register	Values [0...255]: bit field for masking channel pairs 0/1...14/15. A "1" masks channels at bit position.

Bit (Val)	7 (128)	6 (64)	5 (32)	4 (16)	3 (8)	2 (4)	1 (2)	0 (1)
Channels	15 + 14	13 + 12	11 + 10	9 + 8	7 + 6	5 + 4	3 + 2	1 + 0

Test Pulser

118	Pulser on / off	Values 0 / 1 / 2: switches internal test pulser off / 2.5 MHz / 1.22 kHz. 3 uses Veto input to init a pulse. Veto is off

Monitor Outputs

122	Monitor 0	Defines channel for monitor mapping to trigger mask
123	Monitor 1	

Trigger Pattern

124	Pattern 0, low byte	Coincidence trigger pattern 0
125	Pattern 0, high byte	
126	Pattern 1, low byte	Coincidence trigger pattern 1
127	Pattern 1, high byte	

Trigger sources

128	Trigger 0	
129	Trigger 1	
130	Trigger 2	

Gate generator sources

131	Gate Generator	

Multiplicity trigger boundaries

132	Multiplicity low byte	
133	Multiplicity high byte	

Pair Coincidence Pattern

134	Pair pattern 0	
136	Pair pattern 1	
138	Pair pattern 2	
140	Pair pattern 3	
142	Pair pattern 4	
144	Pair pattern 5	
146	Pair pattern 6	
148	Pair pattern 7	
150	Pair pattern 8	
152	Pair pattern 9	
154	Pair pattern 10	
156	Pair pattern 11	
158	Pair pattern 12	
160	Pair pattern 13	
162	Pair pattern 14	
164	Pair pattern 15	

Firmware versions*

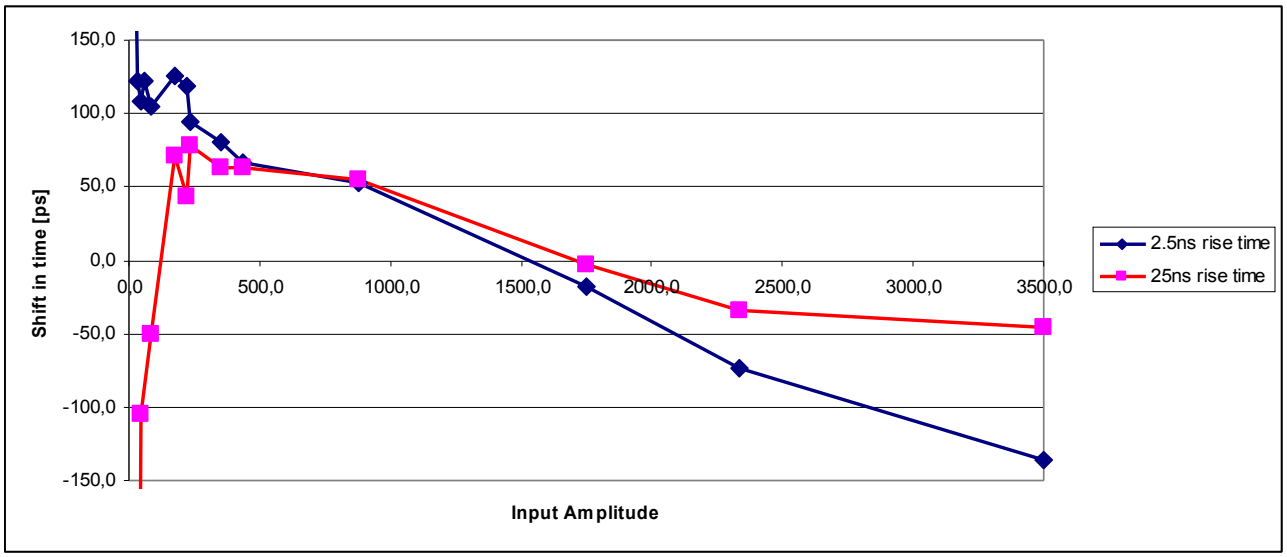
254	FPGA version	16 bit: hi.lo = major.minor
255	CPU version	16 bit: hi.lo = major.minor

* From CPU Firmware 2.18 upwards

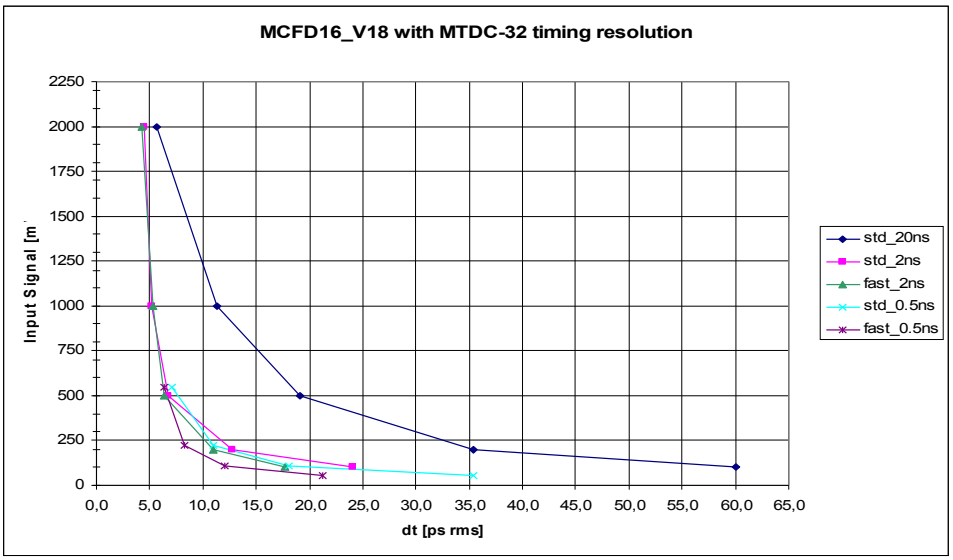
Appendix

Walk

Amplitude dependence of trigger time.
MCFD-16 setting: Gain = 1, Threshold = 5 mV, Tap 1 for 2.5 ns, tap 5 for 25 ns rise time signals, fraction = 20 %.

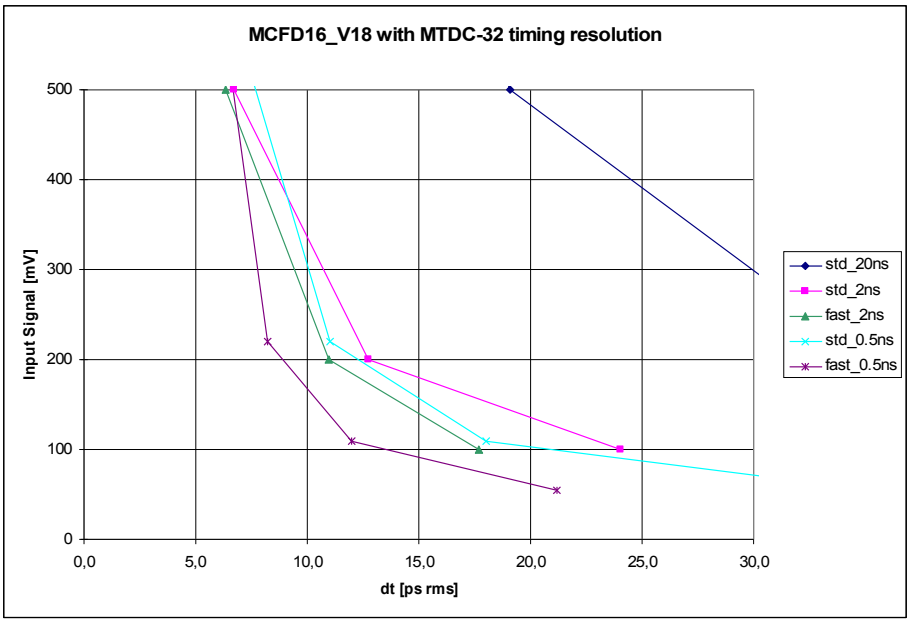


Timing resolution



Measurements were performed with the following setup:
MCFD-16 signal generator connected to channel 0 and 8, A twisted pair cable with 1 m of length connects ECL signals to MTDC-32. Gain = 1, delay chips: 5 ns total delay (5 taps).
The known single channel resolution limit of MTDC 32 is around 4 ps.
The following picture shows the single channel resolution of MCFD-16 in ps rms units.

For MCFD-16 two types are available, standard type and fast type. The fast type provides better timing resolution starting with 2 ns rise time signals and downwards.
It is not recommended for signals slower than 5 ns rise time.



previous diagram Zoomed