Software Module MDPP-32-PADC

V0003

32 channel VME pulse processor

The software module MDPP-32-PADC provides the functionality of a high resolution peak sensing ADC, which also provides a precise time of the sensed pulse maximum.

MDPP-32 with PADC software module:

- **Gain-polarity jumpers**

  determine: termination, polarity, input range and input configuration (differential / uni polar).

  The usual input jumper for PADC are 10V, high Ohmic (1kOhm). But also differential signals and very small signals are possible by selecting a Gain-jumper.

- **Low noise variable gain input amplifiers.**

  The input maximum range can be smoothly adjusted from 10V to 0.5V and beyond (with 10V gain jumpers).

- **Amplitude resolution**

  for 2us FWHM pulses, reaches an rms noise corresponding to a 32 bit ADC.

  Temperature stability at gain = 1, reaches 25ppm/°C

- **AC-coupled and baseline restored**

  Offsets of the input signals have no effect. Even at highest rates, the amplitude keeps stable. Conversion of DC voltage is not possible

- **Dead time / rate capability**

  For input pulse width of more than 400ns there is no additional dead time.

- **Two high resolution monitor outputs**

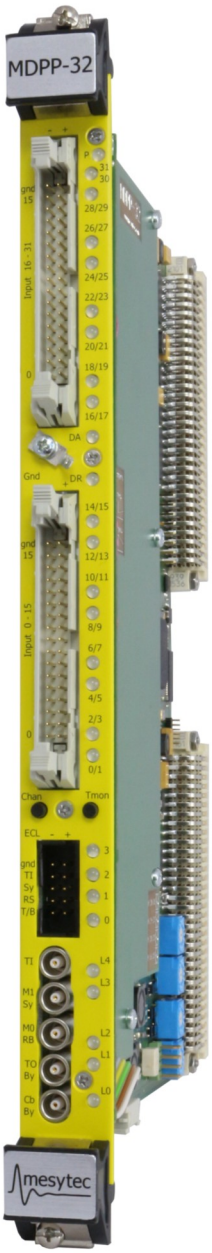
  for monitoring input signals and integrals of signals.

- **Two high resolution trigger inputs**

  24 ps resolution, start window, add time stamp

- **One high resolution trigger output** (1.5 ns resolution)

- **Installation and update via USB**



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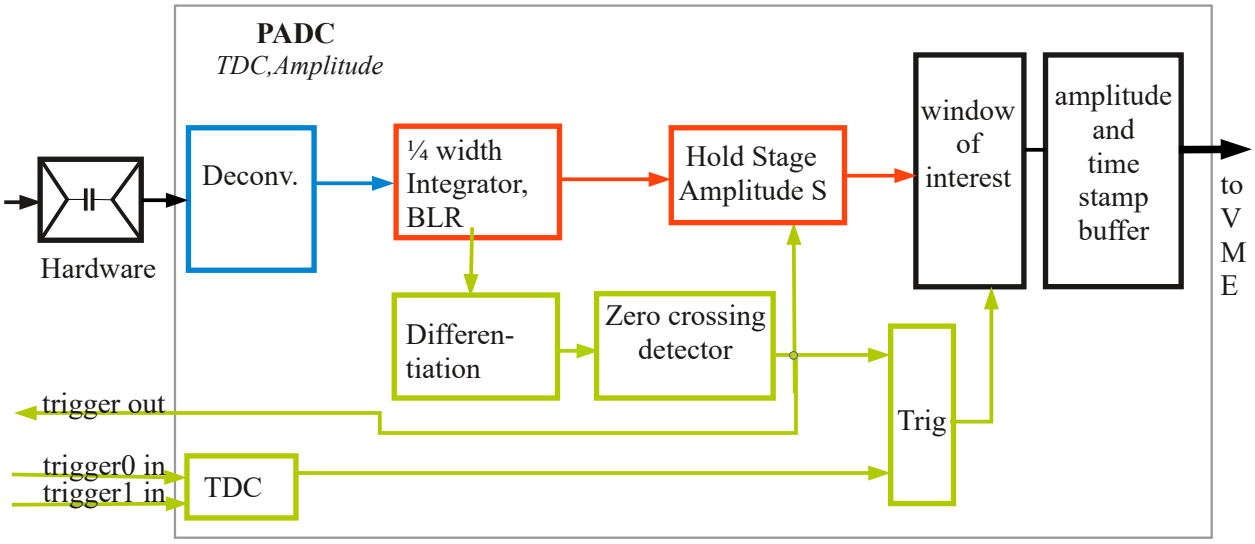
Software module: "PADC"

Delivers timing and very precise amplitude for signals from a shaping amplifiers. It equally processes Gaussean, triangular or trapezoidal signals.
The timing resolution depends on signal to noise ratio and shaping time. It may get down to a resolution of 70ps rms. The channels can be operated self triggered, or an external trigger signal can open a window of interest.

The following picture shows a schematic representation of the software:



The signal is amplified filtered digitized. Then the pre- differentiation is removed by a deconvolution. Then the signal is integrated with a time constant of about ¼ of the FWHW of the signal. This improves the resolution to up to 1/32000 of the full range.
A timing path detects the exact maximum of the peak, and samples it with highest precision (jitter down to 70ps rms).

Then the amplitude and timing values are filtered by a **window of interest** and stored in a **buffer**.

Short data:

- Amplitude resolution of up to 32 k (15 bit)
- Trigger to channel time resolution of **< 70 ps rms,** uniform at any delay.
- Channel to channel time resolution of **< 70 ps rms**, uniform at any delay.
- Trigger input with 24 ps timing resolution
- Can be operated self triggered or externally triggered
- Outputs internal raw trigger with 1.5 ns time resolution

As easy to operate as all mesytec modules and fully data compatible.

Only 4 parameters have to be set:

In Hardware:

Polarity of the signal,
set Jumper to correct position

For the PADC firmware 10V, 1 kOhm jumpers are added, to allow to adjust a maximum range from 0.4V to 10V (by internal gain) without termination. But also the other jumpers can be used.

Register Settings

Signal properties:

1. signal width [ns]
2. Amplifier Gain (can be set from 1 to 25 in steps of 1%).

Analysis property

3. thresholds

Output Data

Amplitude:

channel 0..31 Amplitude 16 bit. Best achievable resolution: 15 bit (1/32000).

Timing: Difference to window start:

channel 32 to 63 channel time difference (16bit)

Chan 64,65 Trigger input 0,1 time diff. (16 bit)

Monitor outputs
(Lemo 2 = mon 0, and Lemo 3 = mon 1)

Switching on the monitor: press pus button "chan", then select a wave form with "Tmon" button. The button "chan" allows to switch through the individual channels.

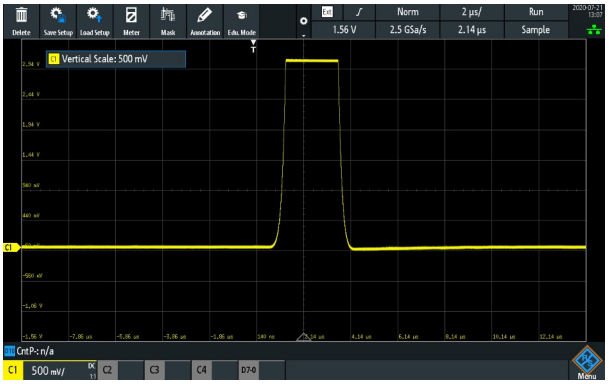
Wave forms:

Tmon 0,
Yellow: mon0, signal at ADC,
Green: trigger output

Tmon 1:
Yellow: mon 0, Signal after deconvolution
Green: Trigger output

Tmon 2 :
Yellow: mon0, integrated, baseline restored signal.
Green: trigger output

Tmon 3: Check **noise**
Yellow: mon 0, integrated baseline restored signal signal amplified by 32.



MDPP-32 register set, PADC Firmware.
Only registers which are different to RCP and SCP software modules are listed.

Data FIFO, read data at address 0x0000 (access R/W D32, 64)

only even numbers of 32 bit-words will be transmitted. In case of odd number of data words, the last word will be a fill word (= 0).

FIFO size: 48kwords - 512words = 48640 words with 32 bit length

Header (4 byte)

2 header signature	2 subheader	4	8 module id	3 TDC_resolution → 0x6042	3 ADC_resolution → 0x6046	10 number of following data words, including EOE
b01	b00	xxxx	module id	bxxx	bxxx	number of 32 bit data words

Data (4 byte) DATA event

2 data-sig	2	4	1	7	16
b00	01	xxxx	overflow	channel number 0..31	Peak ADC value

Data (4 byte) DATA event

2 data-sig	2	5	7	16
b00	01	xxxxx	channel number 32..63	TDC time difference

Data (4 byte) DATA event

2 data-sig	2	5	7	16
b00	01	xxxxx	channel number 64..65	Trigger time difference, T0,T1 External Trigger inputs

Data (4 byte) Extended time stamp

2 data-sig	2	12	16
b00	10	xxxx xxxx xxxx	16 high bits of time stamp

Data (4 byte), fill dummy (to fill MBLT64 word at odd data number)

2 data-sig	30
b00	0

End of Event mark (4 byte)

2	30
b11	event counter / time stamp

Registers

	operation mode				
0x6044	output_format	2	RW	3	0 = time + peak amplitude 1 = peak amplitude only 2 = time only (TDC mode)

Channel addressing (select channel which are set)

0x6100	select_chan_quad	4	RW	8	channel to be modified: 0..7 channel quadruples; 0 = chan 0,1,2,3 1 = chan 4,5,6,7 ... 8 = all channels (set to common values)

Channel settings for quadruples of channels,

****** After writing a register in this page, 20 us wait time is required ********

Address	Parameter				
0x611A	Gain	15	RW	100	100= 1; up to 25000 = 250
0x611C	threshold0	15	RW	255	1...0xFFFF; example: 0.8% = 0x200; **Thresholds have to be set close to noise for good amplitude resolution.**
0x611E	threshold1	15	RW	255	1...0xFFFF; for chan1 in quad
0x6120	threshold1	15	RW	255	1...0xFFFF; for chan2 in quad
0x6122	threshold1	15	RW	255	1...0xFFFF; for chan3 in quad
0x6124	Signal_width		RW	80	2..2000 in multiples of 12.5ns
0x6126	BLR	2	RW	2	0= BLR off, 1= strict, 2=soft

Special Trigger outputs

Starting with March 2021 a new feature is built into all firmware. The VME IRQ lines are mostly unused, but are very good high quality lines to the VME controller. A combination of input triggers can be sent to the 7 available IRQ lines, and can be processed in the Triger IO of the MVLC controller. A collision of signals with other IRQ signaling of the module should be avoided. Several modules may control the same IRQ line, the outputs are then a wired OR of all participating modules. Pulse length is fixed 50ns.

VME-Addr	**Name**	Width	Direction	Value	Description
0x6300	**Trig to IRQ1**	16	RW	0x0000	Connect an OR of the selected channel triggers (0 to 15) to IRQ line 1. Example 0b00000000 10000001 means channel 0 and 7 are Ored and sent to IRQ 1
0x6302	**Trig to IRQ1**	16	RW	0x0000	IRQ1, as above, for channels 16...31
0x6304	**Trig to IRQ2**	16	RW	0x0000	
0x6306	**Trig to IRQ2**	16	RW	0x0000	
0x6308	**Trig to IRQ3**	16	RW	0x0000	
0x630A	**Trig to IRQ3**	16	RW	0x0000	
0x630C	**Trig to IRQ4**	16	RW	0x0000	
0x630E	**Trig to IRQ4**	16	RW	0x0000	
0x6310	**Trig to IRQ5**	16	RW	0x0000	
0x6312	**Trig to IRQ5**	16	RW	0x0000	
0x6314	**Trig to IRQ6**	16	RW	0x0000	
0x6316	**Trig to IRQ6**	16	RW	0x0000	
0x6318	**Trig to IRQ7**	16	RW	0x0000	
0x631A	**Trig to IRQ7**	16	RW	0x0000	

How to set channel parameters

Gain: The internal Gain. Input range is Gain jumper range / gain. For example: Gain jumper is 10V, 1kOhm, expected input signal has maximum 4V, so gain has to be set to 2.5, set value = 250;

Signal_width This is the width of the input pulse at half the peak amplitude in multiples of 12.5ns.

Threshold0/1: The threshold parameter can be set separately for the four addressed channels. Full range is 64k (65535) = 0xFFFF; So a 1% of full range threshold is 65535/100 = 655;

Pulse width: is the full width half maximum value of the shaped input pulse in multiples of 12.5ns. For example: the pulse has a width of 1us, so setting is 1000/12.5 = 80:
The value is internally used to calculate the integration time and to set the BLR.

BLR: the base line restorer can be switched off → = 0. This will degrade resolution, and makes only sense when the signals are very degraded, for example large undershoots..
Settings 2 give a soft response with long time constant, = 1 will restore with shorter time constant. Usually the effect between 1 and 2 will be small.

High precision measurements:

Best temperature stability is with Gain = 1, minor degradation for others.
The pulse FWHM is essential to deliver input for BLR and integration.
Temperature stability 25E-6 /°C @ gain=1;
Differential non linearity TBD (<1%)
Integral non linearity TBD (< 1E-4)

If precision below 1E-4 in INL is required:

INL corrections should be performed after each power up.
(ADCs perform self calibration after each power up)
Wait 15 minutes for thermal equilibrium.
For highest stability Air condition (stable temperature) is useful.